Code : 100305

B.Tech 3rd Semester Exam., 2020
(New Course)

DIGITAL ELECTRONICS

Time : 3 hours *Full Marks* : 70

Instructions :

(i) The marks are indicated in the right-hand margin.

*(ii) There are **NINE** questions in this paper.*

*(iii) Attempt **FIVE** questions in all.*

*(iv) Question No. **1** is compulsory.*

1. Choose the correct answer of the following (any *seven*) : 2×7=14

(a) Dynamic RAM employs

(i) capacitor or MOSFET

(ii) FET or JFET

(iii) capacitor or BJT

(iv) BJT or MOS

(b) The resolution of a 10-bit AD converter for an input range of 10 V is approximately

(i) 1 V

(ii) 1 mV

(iii) 10 mV

(iv) 100 mV

(c) The evolution of PLD begins with

(i) EROM

(ii) RAM

(iii) PROM

(iv) EEPROM

(d) The parameter through which 16 distinct values can be represented is known as

(i) bit

(ii) byte

(iii) word

(iv) nibble

(e) The number of full and half adders required to add 16-bit number is

(i) 8 HA, 8 FA

(ii) 1 HA, 15 FA

(iii) 16 HA, 0 FA

(iv) 4 HA, 12 FA

(f) If we record any music in any recorder, such type of process is called

(i) multiplexing

(ii) encoding

(iii) decoding

(iv) demultiplexing

(g) The no. of D flip-flop required to form a 5-bit ring counter is

(i) 3

(ii) 4

(iii) 5

(iv) None of the above

(h) An overflow is a/an

(i) hardware problem

(ii) software problem

(iii) user-input problem

(iv) input-output problem

(i) The systematic reduction of logic circuits is accomplished by

(i) symbolic reduction

(ii) TTL logic

(iii) Boolean algebra

(iv) truth table

(j) A latch is an example of a/an

(i) monostable multivibrator

(ii) astable multivibrator

(iii) bistable multivibrator

(iv) 555 time

2. (a) Design an excess-3 to BCD code converter using minimum number of NAND gates. 8

(b) Prove the following : 3×2=6

(i) $A \oplus B = \bar{A} \oplus \bar{B}$

(ii) $A \oplus \bar{B} = A \oplus \bar{B} = \bar{A} \oplus B$

3. (a) How can we implement preset and clear inputs in a flip-flop? Explain with the help of a diagram and list their uses. 3+3=6

(b) Design a Mod 9 counter using T flip-flops. 8

4. (a) Explain internal organization of 16×2 memory chips using suitable diagrams. Calculate the maximum rate at which data can be stored and read for a memory having following timing parameters : 4+2=6

Parameter	*Time* (ns)
Read to Output Valid Time (t_{RD})	70
Data Setup Time (t_{DW})	120
Read to Cycle Time (t_{RC})	200
Write Release Time (t_{WR})	0
Write Cycle (t_{WC})	200

(b) Differentiate between Word Capacity and Word Size. Design a 16×8 CAM, using 8×2 CAM chips. 2+6=8

5. (a) Define resolution, linearity, accuracy and settling time of D/A converters. A typical D/A converter has a full-scale analog output of 10 V and accepts 6 binary bits as input. What will be the voltage corresponding to each analog step? 4+2=6

(b) Design a 3-bit parallel comparator A/D converter that provides output in 2's complement format. 8

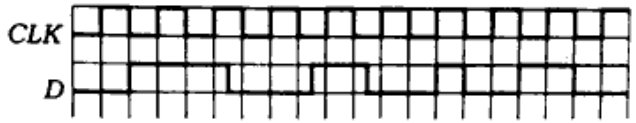
6. (a) Design a BCD to 7-segment display decoder circuit using logic gates. 8

(b) Design full adder using the following : 3×2=6

(i) 8:1 mux

(ii) 4:1 mux

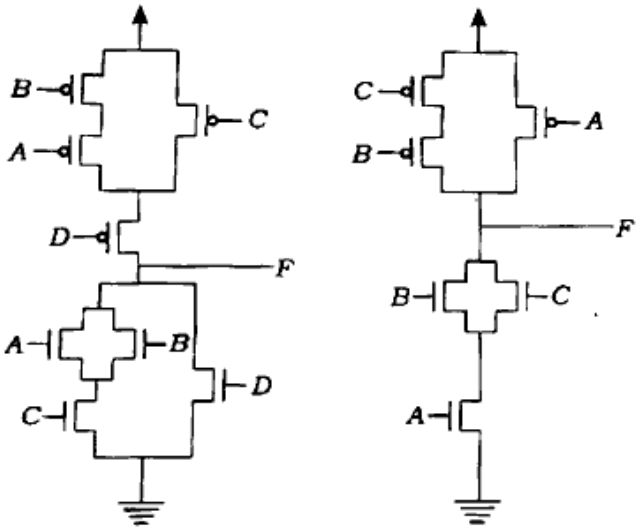
7. (a) On the following graph, inputs *CLK* and *D* are shown :



They are inputs to a *D* latch and a positive edge triggered *D* flip-flop. Assuming initial output 0, draw the output waveform for flip-flop and latch. Do the two outputs differ? If so, why? 2+2+2=6

(b) Explain SIPO and SISO operations of shift register with relevant logic diagrams and truth tables. 8

8. (a) Identify the following logic functions implemented at F : 6



(b) Implement the following CMOS logics : 4×2=8

(i) $\overline{AB(A+B)}$

(ii) $\overline{((CD)+B)A}$

9. (a) What are weighted, non-weighted, cyclic and self-complementary codes? Explain each with examples. 8

(b) Find the values of X in the following conversions : 2×3=6

(i) $(95 \cdot 10)_{10}$ to $(X)_2$

(ii) $(45 \cdot 70)_8$ to $(X)_2$

(iii) $(168 \cdot 16)_8$ to $(X)_{16}$

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