Code : 100303

B.Tech 3rd Semester Exam., 2020
(New Course)

BASIC ELECTRONICS ENGINEERING

Time : 3 hours *Full Marks* : 70

Instructions :

(i) The marks are indicated in the right-hand margin.

*(ii) There are **NINE** questions in this paper.*

*(iii) Attempt **FIVE** questions in all.*

*(iv) Question No. **1** is compulsory.*

1. Answer the following questions (any *seven*) : 2×7=14

(a) Why is negative feedback desired in amplifier application?

(b) Draw the voltage transfer curve of op-amp.

(c) State the Barkhausen's criteria for electronic system to oscillate with feedback.

(d) How is amplifier different from the oscillator?

(e) Why is the reception in the case of amplitude modulation usually noisy?

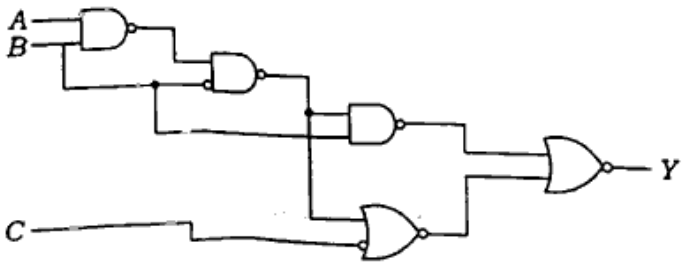
(f) What is cell splitting and how does it increase the capacity of cellular network?

(g) Justify that BJT is current controlled while FET is voltage-controlled device.

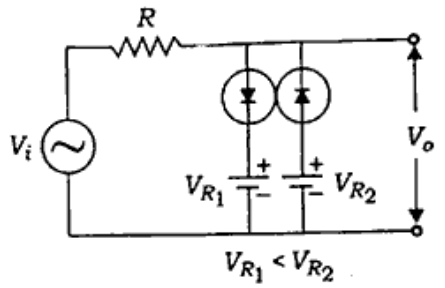
(h) Name the breakdown mechanism in the lightly doped *P-N* junction diode under reverse biased condition.

(i) Why is Gray code also called as reflected code? Convert $(396)_{10}$ to Gray code.

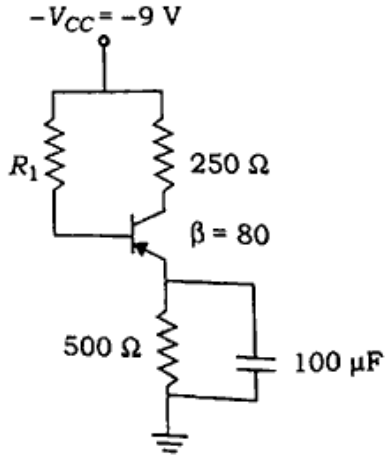
(j) For the logical circuit shown in the figure below, derive the simplified Boolean expression for output *Y* :



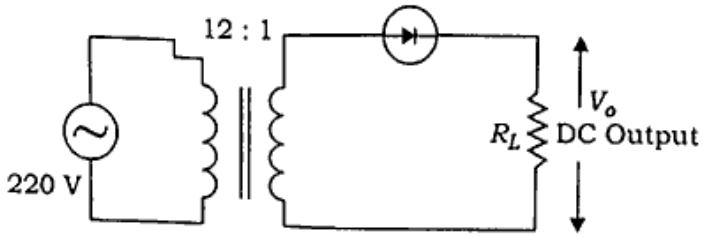
2. *(a)* Draw the waveform of output V_o and explain the operation of circuit in the figure given below : 7



(b) Calculate the value of R_1 in the biasing circuit in the figure given below, so that the Q-point is fixed at $I_C = 8$ mA and $V_{CE} = 3$ V : 7

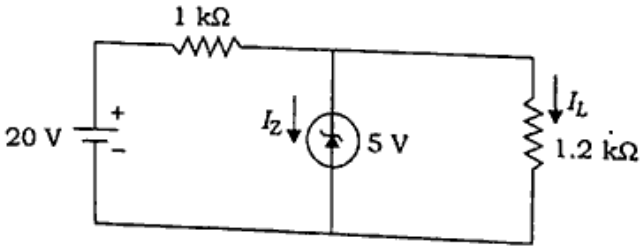


3. *(a)* Calculate the maximum DC voltage and DC current available from a half-wave rectifier shown in the figure given below :



What is the PIV of the diode used in the rectifier? 7

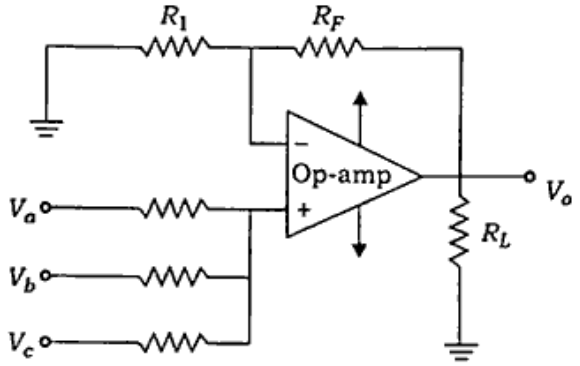
(b) In the figure given below, calculate the load current I_L and Zener diode current I_Z : 7



4. *(a)* Minimize the given Boolean function F using K map in SOP and implement using NAND gate : 7

$$F(A, B, C, D) = AB\overline{C}D + \overline{A}BCD + \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}\overline{D} + A\overline{C} + A\overline{B}C + \overline{B}C$$

(b) The circuit given below is the basic application of op-amp to perform the addition operation :



Explain the operation of circuit and derive the expression of output voltage. 7

5. (a) Design the voltage follower using op-amp and explain the operation. 7

(b) Draw the circuit diagram of voltage-shunt feedback amplifier and derive the expression of closed-loop voltage gain. 7

6. (a) Draw the block diagram of cellular network and briefly explain its operation. 7

(b) Draw the functional block diagram of AM transmitter and receiver. 7

7. (a) Design Schmitt trigger using IC 555 timer and explain its operation with the help of functional diagram. 7

(b) If $R_1 = R_2 = R_3 = 450\ k\Omega$ and $C_1 = C_2 = C_3 = 60\ pF$, determine the frequency of oscillation in phase-shift oscillator. Draw the basic circuit of an *R-C* phase-shift oscillator and explain its operation. 7

8. (a) A new clocked *X-Y* flip-flop is defined with inputs *X* and *Y* in addition to the clock input. The flip-flop functions are as follows :

If $XY = 00$, the flip-flop changes state with each clock pulse. If $XY = 01$, the flip-flop state *Q* becomes 1 with the next clock pulse. If $XY = 10$, the flip-flop state *Q* becomes 0 with the next clock pulse. If $XY = 11$, no change of state occurs with the clock pulse.

Write the truth table and excitation table of *X-Y* flip-flop. Implement the *X-Y* flip-flop using a *J-K* flip-flop. 7

(b) What is the race around condition in *J-K* flip-flop? What are the methods to resolve the race around condition in *J-K* flip-flop? Explain each method with the help of example. 7

9. *(a)* What are the problems with normal encoder? How can these problems be solved by the priority decoder? Design 2 to 4 lines priority encoder. 7

(b) Draw the block diagram of micro-controller and briefly explain each block. 7

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