# Code : 051402

## B.Tech 4th Semester Exam., 2019

## COMPUTER ARCHITECTURE

*Time* : 3 hours *Full Marks* : 70

*Instructions* :

*(i) The marks are indicated in the right-hand margin.*

*(ii) There are* ***NINE*** *questions in this paper.*

*(iii) Attempt* ***FIVE*** *questions in all.*

*(iv) Question No.* ***1*** *is compulsory.*

**1.** Choose the correct answer for any *seven* of the following : 2×7=14

*(a)* How many 128×8 bit RAMs are required to design 32 k×32 bit RAM?

*(i)* 512

*(ii)* 128

*(iii)* 1024

*(iv)* 32

*(b)* The intradata transfer techniques are implemented using

*(i)* serial I/O

*(ii)* parallel I/O

*(iii)* Both *(i)* and *(ii)*

*(iv)* Neither *(i)* nor *(ii)*





*(c)* The sequence of events that happen during a typical fetch operation is

*(i)* PC→MAR→Memory→MDR→IR

*(ii)* PC→Memory→MDR→IR

*(iii)* PC→Memory→IR

*(iv)* PC→MAR→Memory→IR

*(d)* In case of pipelining processor, loop buffer is

*(i)* very high speed memory maintained by the instruction fetch stage

*(ii)* very high speed memory maintained by the instruction decode stage

*(iii)* very high speed memory maintained by the instruction execute stage

*(iv)* None of the above

*(e)* The average memory access time for a machine with a cache hit rate of 90% where the cache access time is 10 ns and the memory access time is 100 ns is

*(i)* 55 ns

*(ii)* 45 ns

*(iii)* 90 ns

*(iv)* 19 ns

(f) The minimum time delay between the initiations of two independent memory operations is called

(i) access time

(ii) cycle time

(iii) transfer rate

(iv) latency time

(g) In case of vectored interrupt, interrupt vector means

(i) the branch information from the source which interrupts the system

(ii) an address that points to a location in memory where the beginning address of the I/O service routine is stored

(iii) Both (i) and (ii)

(iv) None of the above

(h) A microprogrammed control unit

(i) is faster than a hardwired control unit

(ii) facilitates easy implementation of new instructions

(iii) is useful when every small program is to be run

(iv) usually refers to the control unit of the microprocessor





(i) Relative addressing mode is used to write position independent code because

(i) the code in this mode is easy to atomize

(ii) the code in this mode is easy to relocate in the memory

(iii) the code in this mode is easy to make resident

(iv) the code execution faster in this mode

(j) Which of the following holds data and processing instructions temporarily until the CPU needs it?

(i) ROM

(ii) Control unit

(iii) Main memory

(iv) Coprocessor chip

2. (a) How do instruction set, compiler technology, CPU implementation and control, and cache and memory hierarchy affect the CPU performance? Justify the effects in terms of program length, clock rate and effective CPI.

(b) How is virtual memory managed using paging and TLB? Explain with suitable example. 7+7=14

3. *(a)* Explain register reference and memory reference instructions in detail with suitable examples.

   *(b)* Draw the block diagram of control unit of basic computer. Explain in detail with control timing diagrams. 7+7=14

4. *(a)* Explain one-, two- and three-address instruction with suitable examples.

   *(b)* Give an integrated diagram, showing the TLB and cache operations for a logical/virtual address generated by a processor. 7+7=14

5. *(a)* Explain the daisy chaining mechanism for bus arbitration. Analzye the three bus arbitration methods—daisy chaining, polling and independent requesting with respect to communication reliability in the even of hardware failures.

   *(b)* Give the block diagram of microprogram sequencer for a control memory and explain it properly. 7+7=14

6. *(a)* What do you understand by hardwired control? Give various methods to design hardwired control unit. Describe any one with suitable example.





   *(b)* Describe autoincrement and auto-decrement addressing modes with proper examples. 7+7=14

7. *(a)* What is direct memory access? Explain. Give block diagram of circuitry required for direct memory access.

   *(b)* A digital computer has a common bus system of 16 registers of 32 bits each. The bus is constructed with multiplexers.

      *(i)* How many selection inputs are there in each multiplexer?

      *(ii)* What size of multiplexers is needed? 7+7=14

8. *(a)* When do you say the floating point number is normalized? Explain how floating point representation of number is done. Represent the number (+46·25) as floating point binary number with 32 bits.

   *(b)* What are hazards in pipeline architecture? Explain its type with suitable example. 7+7=14

9. (a) What is array processor? Explain SIMD array processor with suitable example.

(b) A DMA controller transfers 16-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at the rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second. By how much will the CPU be slowed down because of DMA transfer? 7+7=14

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