Code : 051602

B.Tech 6th Semester Exam., 2018

COMPUTER ARCHITECTURE

Time : 3 hours *Full Marks* : 70

Instructions :

(i) The marks are indicated in the right-hand margin.

*(ii) There are **NINE** questions in this paper.*

*(iii) Attempt **FIVE** questions in all.*

(iv) Question No. 1 is compulsory.

1. Choose the correct option for each of the following (any *seven*) : 2×7=14

(a) Which among the following can be considered as most advanced ROM?

(i) DRAM

(ii) EEPROM

(iii) RAM

(iv) PROM

(b) Where the results of arithmetic and logical operation are stored?

(i) In accumulator

(ii) In cache memory

(iii) In ROM

(iv) In instruction registry

(c) Which determines the address of I/O interface?

(i) Register select

(ii) Chip select

(iii) Both *(i)* and *(ii)*

(iv) None of the above

(d) Whenever CPU detects an interrupt, what it do with current state?

(i) Save it

(ii) Discard it

(iii) Depends system to system

(iv) First finish it

(e) _____ reads the data by reflecting pulses of laser beams on the surface.

(i) Magnetic disk

(ii) Optical disk

(iii) Floppy disk

(iv) ROM

(f) The instruction, Add#45, R1 does

(i) adds the value of 45 to the address of R1 and stores 45 in that address

(ii) adds 45 to the value of R1 and stores it in R1

(iii) finds the memory location 45 and adds that content to that of R1

(iv) None of the above

(g) The usual BUS structure used to connect the I/O devices is

(i) star BUS structure

(ii) multiple BUS structure

(iii) single BUS structure

(iv) node to node BUS structure

(h) Any condition that causes a processor to stall is called as

(i) hazard

(ii) page fault

(iii) system error

(iv) None of the above

(i) The stalling of the processor due to the unavailability of the instructions is called as

(i) control hazard

(ii) structural hazard

(iii) input hazard

(iv) None of the above

(j) After the completion of the DMA transfer the processor is notified by

(i) acknowledge signal

(ii) interrupt signal

(iii) WMFC signal

(iv) None of the above

2. (a) Define DMA. What is cycle stealing? 7

(b) Why is LRU replacement policy used in block placement from memory to cache? 7

3. (a) Explain all types of cache misses. 6

(b) If memory addresses are 5, 17, 64, 18, 26, 16, 68, 74, 80, 84, 92, 100, 64, 18, 26, 16, block size = 8 byte, 2-way set associative cache and number of sets in cache = 4, find hit percentage and final content of cache. 8

4. (a) What is direct mapped cache? Why is multiplexer needed in direct mapped cache? 5

(b) What is fully associative cache? How set associative cache removes the disadvantages of direct mapped cache and fully associative cache? 9

5. (a) What is interleaved memory? Write two modules of memory access operation. (Hint : Conjugative words in a module, Conjugative words in adjacent module) 8

(b) What is pipelining? How is it better than sequential execution? 6

6. (a) What is data hazard? Write mechanism to reduce data hazard. 7

(b) What is control hazard? Write mechanism to reduce control hazard. 7

7. (a) Differentiate between RISC and CISC. Which one is better? 7

(b) Write the difference between horizontal and vertical microinstructions. 7

8. (a) Why CPU accesses data from primary memory rather than secondary memory? 7

(b) What is the advantage and disadvantage over using multiple cache between RAM and CPU? 7

9. (a) What does the 'reduced' in reduced instruction set computer actually mean? 7

(b) In Flynn's taxonomy—

(i) what does SIMD stand for? Give a brief description and an example;

(ii) what does MIMD stand for? Give a brief description and an example.

3½×2=7

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