Code : 051602

B.Tech 6th Semester Exam., 2019

COMPUTER ARCHITECTURE

Time : 3 hours *Full Marks* : 70

Instructions :

(i) The marks are indicated in the right-hand margin.

(ii) There are ***NINE*** *questions in this paper.*

(iii) Attempt ***FIVE*** *questions in all.*

(iv) Question No. ***1*** *is compulsory.*

1. Choose the correct answer of the following (any *seven*) : 2×7=14

(a) Consider the following register transfer language :

$$R_3 \leftarrow R_3 + M[R_1 + R_2]$$

where R_1, R_2 are the CPU registers and M is a memory location in primary memory. Which addressing mode is suitable for above register transfer language?

(i) Immediate *(ii)* Index

(iii) Direct *(iv)* Displacement

(b) The intra-data transfer techniques are implemented using

(i) serial I/O

(ii) parallel I/O

(iii) Both *(i)* and *(ii)*

(iv) Neither *(i)* nor *(ii)*

(c) A 5-stage pipeline with the stages taking 1, 1, 3, 1, 1 units of time has a throughput of

(i) 1/3 *(ii)* 1/7

(iii) 7 *(iv)* 3

(d) Which memory unit has lowest access time?

(i) Cache

(ii) Registers

(iii) Magnetic disk

(iv) Main memory

(e) The average memory access time for a machine with a cache hit rate of 90%, where the cache access time is 10 ns and the memory access time is 100 ns, is

(i) 55 ns *(ii)* 45 ns

(iii) 90 ns *(iv)* 19 ns

(f) In a 16-bit instruction code format, 3-bit is operation code, 12-bit is address and 1-bit is assigned for address mode designation. For indirect addressing, the mode bit is

(i) 0

(ii) 1

(iii) pointer

(iv) offset

(g) Halt operation comes under

(i) data transfer

(ii) control transfer

(iii) conversion

(iv) I/O transfer

(h) A micro-programmed control unit

(i) is faster than a hardwired control unit

(ii) facilitates easy implementation of new instructions

(iii) is useful when every small program is to be run

(iv) usually refers to the control unit of the microprocessor

(i) Relative addressing mode is used to write position independent code because

(i) the code in this mode is easy to atomize

(ii) the code in this mode is easy to relocate in the memory

(iii) the code in this mode is easy to make resident

(iv) code execution is faster in this mode

(j) Which of the following units can be used to measure the speed of a computer?

(i) SYPS

(ii) MIPS

(iii) BAUD

(iv) None of the above

2. (a) Consider a machine with a main memory of 232 bytes having a direct mapped cache memory of 256 Kbytes with a block size of 8 bytes.

(i) How is the 32-bit address divided into tag, line number and byte number?

(ii) In which line the data corresponding to the address EDCBA987 (H) is sotred?

(b) Give an integrated diagram showing the TLB and cache operations for a logical/ virtual address generated by a processor. 7+7=14

3. (a) Explain the various issues concerning the interrupt processing in computer system. How are multiple interrupt handled and how does processor respond to interrupt request?

(b) What are the hazards in pipeline architecture? Explain its type with suitable example. 7+7=14

4. (a) What is memory interleaving? How is it useful in computer architecture? Explain with suitable example.

(b) A digital computer has a common bus system for 16 registers of 32 bits each.

(i) How many selection inputs are there in each multiplexer?

(ii) What size of multiplexers are needed?

(iii) How many multiplexers are there in a bus? 7+7=14

5. (a) What is overlapped register window? How are window size and register file size computed?

(b) What are the basic differences between a branch instruction, a call subroutine instruction and a program interrupt? 7+7=14

6. (a) What is array processor? Explain SIMD array processor with suitable example.

(b) A DMA controller transfers 16-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at the rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second. By how much will the CPU be slowed down because of DMA transfer? 7+7=14

7. (a) What are pipeline conflicts? Explain the hardware techniques to handle the branch instructions.

(b) Evaluate the arithmetic statement

$$X : (A + B) \times (C + D)$$

using a general register computer with three addresses and two addresses instruction format. 7+7=14

8. (a) What do you mean by asynchronous data transfer? Explain strobe controlled and handshaking mechanism for asynchronous data transfer.

(b) What do you mean by cache memory? How does it affect the performance of the computer system? An eight-way set-associative cache is used in a computer in which the real memory size is 232 bytes. The line size is 16 bytes, and there are 210 lines per set. Calculate the cache size and tag length. 7+7=14

9. (a) What is addressing mode? Why do computers use addressing mode techniques? Explain two modes with examples, which do not use address fields.

(b) List the important characteristics of RISC architecture and explain the use of overlapped register windows. 7+7=14

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